Three-dimensional Integration Demands Multi-dimensional Test and Inspection Strategies

Three-dimensional (3D) integration is becoming a reality. It allows closer coupling between microprocessors and graphics processors and the increasingly large working memories they need. It helps the accelerometers, microphones, and other MEMS devices in the newest smartphones to fit inside a slim, pocket-friendly form factor. It reduces circuit board area and cuts signal transmission times.

But how do you make it all work? Each layer of a 3D stack represents another device to test and another layer-to-layer bond that must be sufficiently uniform and correctly aligned. A bad bond can mean that all of the wafers in the stack have to be scrapped. Building a bad memory chip into a stack might mean that the underlying processor is lost, too.

As Paul Lindner, EVG's executive technology director, explained, many wafer-level integration schemes require both temporary and permanent wafer bonds: between a device wafer and a carrier substrate or between the device wafers in a stack. Each of these bonds requires a uniform adhesive thickness with no voids and minimal warpage.

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The approach EVG recommends depends on silicon carrier substrates. These are readily available, well-characterized, and naturally have the same thermal and mechanical properties as the silicon device wafer. They are, however, opaque to the optical measurements usually used for bond metrology. Instead, the company's Gemini fully-automated bonding system uses infrared to measure the thickness of the adhesive layer. The system scans the entire wafer and can inspect 45 wafer bonds per hour, fast enough for 100% inspection.

Infrared imaging is also useful for lithographers. In the via-last process flow typically used for image sensors, the through-silicon-via (TSV) mask must align to the bonded interface, which means the aligner must be able to see it. Lindner said that EVG has demonstrated 1-micron alignment between the front and back side — more than adequate when these TSV are typically 20 to 80 microns across. The aligner uses reflective IR microscopy to see through the silicon carrier wafers; transmissive microscopy can be difficult because of the presence of doping variations and surface metallization on the device wafer.

While bond metrology can help ensure a good mechanical and electrical connection between two stacked wafers, it's up to final test to make sure that the two devices actually function as a unit. Unfortunately, as Microprobe CEO Mike Slessor explained, 100% testing of every chip in every stacked module is simply not feasible. Each device may require a different test strategy. Indeed, since individual component die may come from different fabs run by different companies, the test strategy must span the entire supply chain.

Just as the purpose of wafer sort is to avoid the expense of packaging non-functional die, Slessor said, the purpose of testing component die is to limit costs at the 3D integration stage. For example, in a stack containing both memory and a microprocessor, the microprocessor represents most of the cost. It therefore might make sense to test the memory devices more exhaustively to avoid the loss of a good processor. Not all examples are so straightforward, though. Often, the individual component die are all complex. In such a case, the pre-bond testing might need to resemble more comprehensive final testing, rather than wafer sort-style screening.

Slessor expects that the test strategy for 3D integrated devices will come to resemble the kind of sampling model seen in front-end wafer inspection. Manufacturers will need to determine the ROI and build a business case for their testing strategy, making sure they test just enough to minimize post-packaging failures. As a result, he said, the rise of 3D integration will not necessarily produce a surge in test equipment sales. Rather, the distribution of test and measurement spending is likely to change.

A 3D module supplier might test externally-sourced components differently from those of its own fab. Accordingly, Microprobe's probe card architecture allows testing at multiple points in the process flow. By changing the probe tip design, the same card design can be used for probing on under-bump metallization, on copper pillars, or on solder caps. Copper pillars in particular are rapidly becoming the most popular flip-chip attachment method: Microprobe announced Tuesday (July 12) that they have shipped more than 1000 Vx and Mx vertical MEMS probe cards for copper pillar applications.

For both test and inspection equipment, it's clear that 3D integration extends the boundaries of process control beyond the walls of the wafer fab. Sessions at TechXpot North Two will look at packaging and test issues associated with 3D integration. On Wednesday afternoon in particular, the Test in Transition session examines test strategies and technologies.

- Katherine Derbyshire